WHAT IS CLAIMED IS:

1. A computer implemented process of performing design for testability analysis and synthesis in an integrated circuit design, comprising the steps of:

partitioning each logic block in an integrated circuit design based on one or more boundaries of multi-cycle initial setup sequence;

excluding the one or more logic blocks with multi-cycle initial setup sequence from valid candidate blocks;

selecting a constraint setting set;

applying the set of constraint setting to the integrated circuit design; and

performing design for testability analysis and synthesis on the valid candidate blocks.

2. The process of claim 1 wherein the steps of selecting and applying the constraint setting set includes:

extracting a subset of constraint settings from the selected constraint setting set; and

applying the extracted subset of constraint settings to the integrated circuit design.

3. The process of claim 1 wherein the step of performing design for testability analysis and synthesis includes performing Static Timing Analysis (STA) based design for testability analysis and synthesis on the valid candidate blocks.

4. The process of claim 1 wherein the step of partitioning includes:

for each logic block in the integrated circuit design,

determining whether the logic block includes a multi-cycle initial setup sequence;

including the logic block in the valid candidate blocks if the block does not include a multi-cycle initial setup sequence, and if the logic block includes the multi-cycle initial setup sequence, determining whether design partition is allowed between the logic block and other blocks in the integrated circuit design; and

excluding the logic block in the valid candidate blocks if design partition is allowed, otherwise, if the design partition is not allowed, including the logic block from the valid candidate blocks.

5. The process of claim 4 wherein when it is determined that the design partition is allowed, extracting and storing one or more internal or external fanin constraints and affected fanout object values.

6. The process of claim 4 wherein when it is determined that the design partition is not allowed, collecting the affected fanout object values when the logic block is in a stable test mode state after the multi-cycle initial setup sequence.

7. The process of claim 1 wherein the step of selecting the constraint setting set includes selecting one of only external object constraint setting being allowed, only internal object constraint setting being allowed, and both internal and external object constraint settings being allowed.

8. The process of claim 1 wherein the applying step further includes the step of initiating the integrated circuit design to enter a stable test mode state with the multi-cycle setup.

9. A computer implemented process for performing class and cell selection procedure in scan cell replacement for an integrated circuit design, comprising the steps of:

encoding a cell to be replaced with a corresponding scan cell;

encoding the scan cell;

determining a cost function between the encoded cell and the encoded scan cell; and

establishing an affinity between the cell and the corresponding scan cell based on the cost function.

10. The process of claim 9 wherein the steps of determining the cost function and establishing the affinity include:

determining a Hamming distance between the encoded cell and the encoded scan cell; and

establishing an affinity between the cell and the corresponding scan cell based on the determined Hamming distance.

11. The process of claim 9 wherein the scan cell includes a dual scan cell, and further, wherein the cell includes a scan cell to which corresponds the dual scan cell.

12. A computer implemented process for performing scan cell replacement for an integrated circuit design, comprising the steps of:

performing class selection from a cell library and gate-level netlist based on affinity between cells;

determining a target characterization for the scan cell replacement; and

replacing one or more cells with a corresponding one or more scan cells having the closest target characteristics.

13. The process of claim 12 wherein the target characteristics include one or more of timing, area, power and/or other metrics.

14. The process of claim 12 wherein the target characteristics include timing-based metrics.

15. The process of claim 14 wherein the step of determining the timing characterization includes selecting one of a static timing characterization and a dynamic timing characterization.

16. The process of claim 15 wherein when the static timing characterization is selected, the scan cell with timing characteristics that is closest to the corresponding cell is selected based on library cell timing data.

17. The process of claim 15 wherein the dynamic timing characterization includes one or more of cell delay and context delay, the context delay including transition delay and connection delay.

18. The process of claim 16 wherein the library cell timing data includes one or more of a constraint type timing arc and a delay type timing arc.

19. The process of claim 18 wherein the constraint type timing arc corresponds to timing constraints between pins, and further, wherein the delay type timing arc corresponds to timing delay between two pins.

20. A computer implemented process of performing design for testability analysis and synthesis in an integrated circuit design, comprising the steps of:

partitioning each logic block in an integrated circuit design based on one or more boundaries of multi-cycle initial setup sequence;

excluding the one or more logic blocks with multi-cycle initial setup sequence from valid candidate blocks;

selecting a constraint setting set;

applying the set of constraint setting to the integrated circuit design;

performing design for testability analysis and synthesis on the valid candidate blocks; and

performing affinity-based scan cell replacement.

21. The process of claim 20 wherein the steps of selecting and applying the constraint setting include:

extracting a subset of constraint settings from the selected constraint setting set; and

applying the extracted subset of constraint settings to the integrated circuit design.

22. The process of claim 20 wherein the step of performing scan cell replacement includes the steps of:

performing class selection from a cell library and gate-level netlist based on affinity between cells;

determining a target characterization for the scan cell replacement; and

replacing one or more cells with a corresponding one or more scan cells having the closest target characteristics.

23. The process of claim 22 wherein the target characteristics include one or more of timing, area, power and/or other metrics.

24. The process of claim 22 wherein the target characteristics include timing-based metrics.

25. The process of claim 20 wherein the step of partitioning includes:

for each logic block in the integrated circuit design,

determining whether the logic block includes a multi-cycle initial setup sequence;

including the logic block in the valid candidate blocks if the block does not include the multi-cycle initial setup sequence, and if the logic block includes the multi-cycle initial setup sequence, determining whether design partition is allowed between the logic block and other blocks in the integrated circuit design; and

excluding the logic block in the valid candidate blocks if design partition is allowed, otherwise, if the design partition is not allowed, including the logic block from the valid candidate blocks.

26. The process of claim 20 wherein the step of selecting the constraint setting set includes selecting one of only external object constraint setting being allowed, only internal object constraint setting being allowed, and both internal and external object constraint settings being allowed.

27. The process of claim 20 wherein the applying step further includes the step of initiating the integrated circuit design to enter a stable test mode state with the multi-cycle setup.

28. A computer program product, comprising:

a medium readable by a computer, the computer readable medium having computer program code adapted to:

partition each logic block in an integrated circuit design based on one or more boundaries of multi-cycle initial setup sequence;

exclude the one or more logic blocks with multi-cycle initial setup sequence from valid candidate blocks;

select a constraint setting set;

apply the set of constraint setting to the integrated circuit design; and

perform design for testability analysis and synthesis on the valid candidate blocks.

29. The process of claim 19 wherein the steps of selecting and applying the constraint setting set include:

extracting a subset of constraint settings from the selected constraint set; and

applying the extracted subset of constraint settings to the integrated circuit design.

30. The computer program product of claim 28, wherein the computer program code is further adapted to perform affinity-based scan cell replacement.